Application Note

DP83TD510E Cable Diagnostics Toolkit

ABSTRACT

With the IEEE 802.3cg 10BASE-T1L standard, engineers can expand the cable reach of their applications beyond what was previously possible – enabling new opportunities for long-distance Ethernet communications. To achieve this longer reach, however, engineers still have to contend with cable faults and degradation, which can lead to costly and labor-intensive troubleshooting and repair. 10BASE-T1L Ethernet PHYs such as the DP83TD510E provide a wide array of cable diagnostic tools to monitor cable performance and provide the longest cable reach. This application note highlights features of the PHY for detecting fault and monitoring link quality in real time.

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The DP83TD510E offers cable diagnostic tools to assist in system design and insitu monitoring. Cable diagnostic tools allows designers to quickly bring-up their systems, evaluate the quality of link between PHYs, and effectively identify cable faults. By enabling the PHY to provide valuable information about the cable and link, designers can have confidence that their systems are robust before deployment. The diagnostic data enables engineers to evaluate the health of their system over time and take action to avoid failures and down-time.

Cable diagnostic tools included in the DP83TD510E:

- Time-Domain Reflectometry (TDR)
- Active Link Cable Diagnostic (ALCD)
- Signal Quality Indictor (SQI)
- Loopback modes
- Pseudo-random binary sequence (PRBS) generator and checker
- IEEE 802.3cg PMA compliance test modes

The following sections will discuss each of these features or tools. Each section will provide background into the functionality of the PHY, instructions on how to configure each item, and procedure for how to analyze the data retrieved. Example scripts are included for each item, and can be used with the USB-2-MDIO software tool for easy evaluation.

2 1-V and 2.4-V p2p Mode Scripts

The default operating modes depend on the strapping the LED_2 pin. From the quick setup in the previous session, the default output operating mode will be 1.0 Vpp with and without a link partner detected.

Select the output operating mode of the DP83TD510E by running the script below for 2.4 Vpp for both link partners.

```
//Set Output operating mode for 2.4 Vpp
begin
08F6 1000 //enable 2.4Vpp operating mode
020E B000 //Request increased the transmit level
001F 4000 //Software restart
end
```

Select the output operating mode of the DP83TD510E by running the script below for 1 Vpp for both link partners.

```
//Set Output operating mode for 1 Vpp
begin
08F6 0000 //enable 1Vpp operating mode
020E 8000 //Do not request increased transmit level
001F 4000 //Software restart
end
```

3 Time-Domain Reflectometry

3.1 TDR Application Startup

The primary cable faults in Ethernet applications are open and short circuit conditions. The 802.3cg standard states that a PHY can withstand open and short circuits without sustaining damage, up to 60 V. The DP83TD510E implements TDR to identify open and short conditions in the cable and to identify the distance from the PHY the cable fault occurs.

Note

TDR cannot be run while the PHY is actively linked to a link partner. TDR works by injecting high energy pulses into the cable and measuring the reflected signal. Activity on the channel will interfere with the transmitted pulses and corrupt the received signal.

3.1.1 TDR_CFG (Address = 0x001E) [Reset = 0x0000]

Table 3-1. TDR_CFG (Address = 0x001E) [Reset = 0x0000]

Bit	Field	Type	Reset	Description
15	TDR_Start	R	0x0	1b = Start TDR procedure
14	CFG_TDR_Auto_Run	R	0x0	1b = Enable TDR auto start on link down
				0b = TDR is manually enabled by default configuration
13:2	Reserved	R	0x0	
1	TDR_Done	R	0x0	1b = TDR completed
				0b = TDR in progress
0	TDR_Fail	R	0x0	1b = TDR failed to complete properly
				0b = No error indication

3.1.2 TDR_Fault_Status (Address = 0x030C) [Reset = 0x0000]

Table 3-2. TDR_Fault_Status (Address = 0x030C) [Reset = 0x0000]

Bit	Field	Type	Reset	Description
15:12	Reserved	R	0x0	
11	Peak_Detect	R	0x0	1b = Fault detected
				0b = No fault detected
10	Peak_Sign	R	0x0	1b = Open fault
				0b = Short fault
9:0	Peak_Location	R	0x0	Fault Location in meters

Note

Bit 0x030C[10] is valid if 0x030C[11] is set (‘1b)

3.2 TDR Test Procedure

Note

Scripts provided in this application note follow the format of the USB-2-MDIO tool. Example: 0301 2404 The first 4-digit value is register address to read or write. The second 4-digit value is register data to write into the address.

To configure the TDR circuitry within the PHY, the following registers must be set:

```
begin
001F 8000
0200 0000
0834 4000
0301 2403
0303 043E
030E 2520
001F 4000
end
```

Start TDR manually:

```
begin
//Soft Reset
001F 4000

//Start TDR measurement
001E 8000
end
```

Check the completion status and results of TDR measurement:

```
begin
//Soft Reset
001F 4000

// Error Checking
001E      //Observe bits [1:0] for completion status, bit [0] must be 1b for TDR status to be valid

//Read TDR result
030C     //Observe bits [11:10] for fault detection and [9:0] for fault location
end
```

The location of the fault is measured in meters and can be found by converting bits 0x030C[9:0] to decimal format.

Note

A High Attenuation cable might need a different TDR script. A Register 030C reading of 0000 indicates that the cable is a high attenuation cable.

4 Active Link Cable Diagnostics

4.1 ALCD Application Startup

While TDR offers a way to measure cable length of a system without an established link, Active Link Cable Diagnostic (ALCD) allows the PHY to determine the cable length during an active link with its link partner. The PHY uses passive digital signal processing along with pre-defined cable parameters to achieve the highest accuracy in its cable length estimate. The estimated cable length can be cross verified with the physical length of the cable to determine whether there is deviation in cable characteristics and understand how the PHY may perform as the cable ages.

It is important to note that in single-pair Ethernet applications, cable selection varies more widely than in standard Ethernet applications (where CAT5, CAT5e, CAT6 cables are dominantly used). As such, the ALCD feature in the DP83TD510E allows designers to tailor their cable diagnostic tool to the specific cable in their application to generate the most accurate cable length estimate.

The ALCD usage is divided into two steps:

1. Calibration of the cable characteristics
2. Measurement of the cable quality

4.2 ALCD Test Procedure

4.2.1 Cable Calibration

The ALCD will need to be calibrated to each cable type and application by measuring the ALCD register information at five regular intervals up to the maximum cable reach the application requires. The calibration can be done in a designer's lab during product evaluation. A good cable will not deviate much in its characteristics from the test cable used in calibration to those deployed in the field, allowing calibration to be performed once for a PHY-cable pair. To perform the calibration and estimate the cable reach of a link, follow the following procedure.

1. The maximum cable length expected to be used in the field with DP83TD510E Ethernet PHY is referred to as maximum operating length with the Ethernet PHY. For example, if 900 m is expected to be the longest cable length which will be used in the field, then 900 m is called as the maximum operating length. ALCD will have reference data for the maximum operating length with some margin for degradation in the cable performance over time. The margin can be fixed (say 10%) or can be derived from the performance with the higher cable length. For the example we can assume a 10% margin and generate reference data for approximately 1 km. It will be referred to as ALCD range.
2. The ALCD calibration is done in five segments of ALCD cable range. It is recommended that these segments are equal or nearly equal in length. For example, we can use either of the following cable lengths for calibrating ALCD or any other set close to these values for ALCD range of 900m. Do keep in mind that the longest cable length for calibration needs to be greater than actual used cable.

   Set 1: {0m, 200m, 400m, 600m, 800m, 1km}
3. An ALCD metric is calculated by the PHY for each segment of the ALCD cable range. It is internally generated by the silicon and is displayed in register 0x0A9D after the link up is achieved. Follow the procedure below to read the correct value of the ALCD metric at each segment length.
   a. Program with a desired script if necessary, and let the devices link up.
   b. Wait for 3ms after the link up is achieved and read register 0x0A9D for the ALCD metric.
   c. Ignore the LSB hexadecimal digit, and store the 3 MSB hexadecimal digits of the metric.
   d. Repeat steps a. through c. for all cable lengths in the calibration set to obtain a calibration pair for 1 V mode and 2.4 V mode.
4. Once the ALCD reference metric is recorded for each cable length, these values can be stored in the DP83TD510E registers to estimate the length of the cable over the lifetime of the application. Six pairs of <cable, metric> are required to be generated following the procedure described above. This information needs to be stored in registers as per Table 4-1 and needs to be part of initial link up script.

Table 4-1. Register Mapping for ALCD Calibration Results

Parameter	Register Address	Comments
2p4V Metric1	0x088D	3 MSB hexadecimal digits for metric 1 for 2p4V mode
2p4V Metric2	0x088E	3 MSB hexadecimal digits for metric 2 for 2p4V mode
2p4V Metric3	0x088F	3 MSB hexadecimal digits for metric 3 for 2p4V mode
2p4V Metric4	0x0890	3 MSB hexadecimal digits for metric 4 for 2p4V mode
2p4V Metric5	0x0891	3 MSB hexadecimal digits for metric 5 for 2p4V mode
2p4V Metric6	0x0892	3 MSB hexadecimal digits for metric 6 for 2p4V mode
1V Metric1	0x0898	3 MSB hexadecimal digits for metric 1 for 1p0V mode
1V Metric2	0x0899	3 MSB hexadecimal digits for metric 2 for 1p0V mode
1V Metric3	0x089a	3 MSB hexadecimal digits for metric 3 for 1p0V mode
1V Metric4	0x089b	3 MSB hexadecimal digits for metric 4 for 1p0V mode
1V Metric5	0x089c	3 MSB hexadecimal digits for metric 5 for 1p0V mode
1V Metric6	0x089d	3 MSB hexadecimal digits for metric 6 for 1p0V mode
Cable1	0x08E9	Round(Cable1/8) and convert it to hexadecimal digits
Cable2	0x08EA	Round(Cable2/8) and convert it to hexadecimal digits
Cable3	0x08EB	Round(Cable3/8) and convert it to hexadecimal digits
Cable4	0x08EC	Round(Cable4/8) and convert it to hexadecimal digits
Cable5	0x08ED	Round(Cable5/8) and convert it to hexadecimal digits
Cable6	0x08EE	Round(Cable6/8) and convert it to hexadecimal digits

Note

Register information is not retained over power cycles. ALCD calibration information should be included in an initialization routine to be available for cable length estimation after each power-up.

The longest cable length for calibration must be greater than actual cable used .

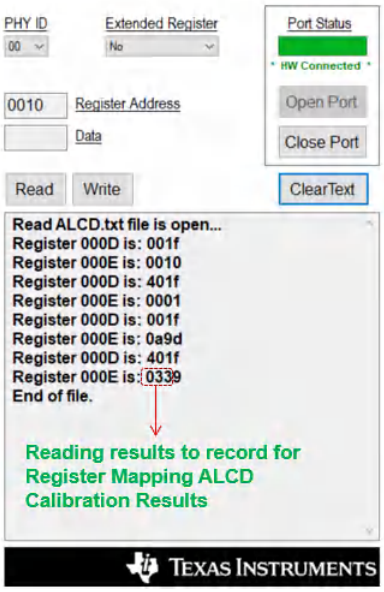

Figure 4-1. Example Reading For Calibration

Procedure to generate ALCD metric:

```
//For each output operating mode utilized in an application, record ALCD <cable, metric pair>

1.0 Vpp operating ALCD metrics
//For each cable length segment in ALCD range, record the ALCD metric
begin
0001 //check that link is established in 0x0001[2]
0A9D //read register 0x0A9D and record bits [15:4] for
end

2.4 Vpp operating ALCD metrics
//For each cable length segment in ALCD range, record the ALCD metric
begin
0001 //check that link is established in 0x0001[2]
0A9D //read register 0x0A9D and record bits [15:4] for
end
```

Set ALCD calibration registers during initialization routine:

```
begin
//Set ALCD cable length segments
08E9 0000 //Cable length 1 is 0 meters
08EA 0019 //Cable length 2 is 200 meters ([200 meters / 8] -> converted to hex)
08EB 0032 //Cable length 3 is 400 meters ([400 meters / 8] -> converted to hex)
08EC 004B //Cable length 4 is 600 meters ([600 meters / 8] -> converted to hex)
08ED 0064 //Cable length 5 is 800 meters ([800 meters / 8] -> converted to hex)
08EE 007D //Cable length 6 is 1000 meters([1000 meters / 8] -> converted to hex)

//Set 1.0 Vpp ALCD metrics
0898 0046 //ALCD metric for 0 meters is 046
0899 0067 //ALCD metric for 200 meters is 067
089A 0088 //ALCD metric for 400 meters is 088
089B 0137 //ALCD metric for 600 meters is 137
089C 0178 //ALCD metric for 800 meters is 178
089D 0263 //ALCD metric for 1000 meters is 263

//Set 2.4 Vpp ALCD metrics
088D 0078 //ALCD metric for 0 meters is 078
088E 0096 //ALCD metric for 200 meters is 096
088F 0120 //ALCD metric for 400 meters is 120
0890 0174 //ALCD metric for 600 meters is 174
0891 0201 //ALCD metric for 800 meters is 201
0892 0310 //ALCD metric for 1000 meters is 310
end
```

4.2.2 Cable Quality Measurement

When the cable calibration is complete, any link over the cable can be measured to estimate the length of the cable.

1. Ensure that the ALCD reference metrics for the cable have been collected and stored in the registers described in Table 4-1.
2. Read register 0x0A9F for the estimated cable length of the link, provided in meters.

```
begin
0A9F //bit[15] indicates ALCD length estimation is complete, bits[10:0] store the estimated cable
length in meters
end
```

Note

Use 2.4V p2p mode to give a more accurate result when estimating the cable length for ALCD.

5 Signal Quality Indicator

5.1 SQI Application Startup

While TDR can provide information about the existence and location of cable faults, a real time monitor of the link quality can provide valuable information before a fault occurs. The DP83TD510E provides real time signal-to-noise ratio monitoring.

The cable quality, connector contact, and surrounding environment contribute to the overall channel quality. The Signal Quality Indicator (SQI) can provide insight into the physical connections in an application assembly before it ships, the link quality of a system in noisy environments and immunity testing, or the lifetime trend a of product's health as it ages.

The DP83TD510E monitors link quality by measuring the SNR at periodic intervals whenever an active link is established. The PHY measures the accumulated mean-square error (MSE) in the received signal at the PAM3 slicer from its sliced output level. The signal quality monitoring functions are run automatically in the background of the PHY; there is no need to enable this feature through register settings.

The MSE stored as a hexadecimal value in the SQI register [0x0A85] can be converted to dB by dividing by 2^{17} and calculating MSE (dB) = 10 * $\log_{10}$ MSE

1. Convert bits [14:0] to decimal form for MSE (decimal)
2. MSE (dB) = 10 * $\log_{10}$ (MSE/2^{17})
3. SNR(dB) = -10 * $\log_{10}$ (MSE/2^{17}) - 1.76 dB

5.1.1 MSE Detection (Address = 0x0A85) [Reset = 0x0000]

Table 5-1. MSE Detection (Address = 0x0A85) [Reset = 0x0000]

Bit	Field	Type	Reset	Description
15:0	MSE Detect	R	0x0	Signal Quality Indication of Link

5.2 SQI Test Procedure

Read MSE detection register for 16 bit MSE value:

```
begin
0x0A85
end
```

Evaluate the health of the link according to Table 5-2:

Table 5-2. SQI Link Health

SQI Link Health	MSE	SNR (dB)
Poor	Mse > 0660h	SNR < 17.29
Marginal	0660h >= Mse > 0320h	17.29 < SNR < 20.38
Good	Mse <= 0320h	SNR > 20.38

6 Cable Diagnostics Summary

With multiple cable diagnostic tools to choose from in the DP83TD510E, selecting the right tool for an application is important. The Table 6-1 offers information about when each tool can be used to detect faults and improve system performance.

Table 6-1. Cable Diagnostic Summary

Application Use Case	Cable Diagnostic Tool		
	TDR	ALCD	SQI
Link Down	Yes	No	No
Network Link Established	No	Yes	Yes
Link segment length	Yes	Yes	No
Open/Short detection	Yes	No	No
Link quality monitor	No	No	Yes

7 Loopback Modes

There are several loopback options within the DP83TD510E that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83TD510E may be configured to any one of the Near-End Loopback modes or to the Far-End (reverse) Loopback mode. MII Loopback is configured using the Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016).

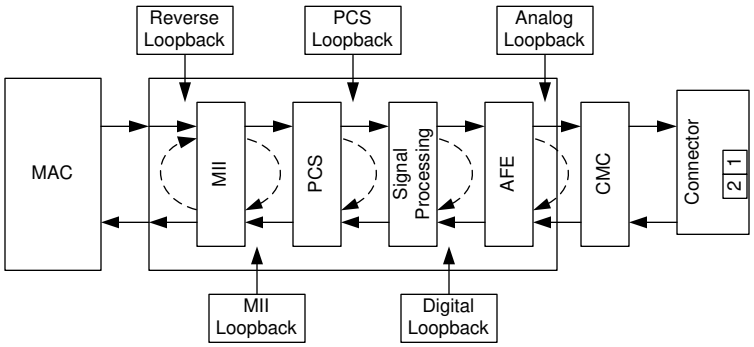

Figure 7-1. Loopback Test Modes

7.1 BISCR (Address = 0x0016) [Reset = 0x0100]

Table 7-1. BISCR (Address = 0x0016) [Reset = 0x0100]

Bit	Field	Type	Reset	Description
6:0	Loopback_Mode	R/W	0x0	0000001b = Reserved 0000010b = PCS loopback (Tx PAM3 to Rx PAM3) 0000100b = Digital loopback 0001000b = Analog loopback 0010000b = Reverse loopback 0100000b = Transmit to MAC in reverse loopback 1000000b = Transmit to MDI in MAC loopback

8 Pseudo-Random Bit Sequence Functions

The DP83TD510E incorporates a Pseudo-Random Bit Sequence (PRBS) generator and checker to allow for Built-in Self-Test (BIST), as well as a cable diagnostic tool. The PRBS circuity can be utilized for internal loopback modes or to send data over the MAC or MDI interfaces. The PRBS simulates pseudo-random data transfer scenarios in the format of real packets and Inter-Packet Gap (IPG) on the lines. The PRBS allows the designer control over the packet length and IPG to simulate expected throughputs of the application. The PRBS is implemented with independent transmit and receive paths, with the transmit block capable of generating a continuous stream of a pseudo-random sequence.

The receive status of whether the PRBS checker is locked to the incoming bit stream, whether the PRBS has lost sync, and whether the packet generator is busy, can be read from the PRBS_STATUS_4 register (0x011F). While the lock and sync indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the PRBS_STATUS_4 register. The number of received packets is stored in PRBS_STATUS_2 (0x011D).

Note

Note: The value stored in any PRBS packet or byte counting register is updated when a write is made to register 0x011F bit[0] or bit[1].

The PRBS test can be put in a continuous packet generation mode by using the PRBS_CFG_1 register (0x0119). In continuous mode, when one of the PRBS counters reaches the maximum value, the counter starts counting from zero again.

```
Enable continuous PRBS generator:
Begin
//Enable continuous PRBS generator/checker over Copper TX/RX
//Note the link partner should be in reverse loopback mode for PRBS checker to have data stream to
evaluate
0119 0557
End
PRBS receive data checker:
Begin
//Write 0x011F[0] to latch packet, error counter values
011F 0001
//Read 0x011F for generator status, sync lock, bit errors
//0x011F = 0x0B00 is indicative of PRBS lock and no errors, passing result
011F
End
```

8.1 PRBS_CFG_1 (Address = 0x0119) [Reset = 0x0574]

Table 8-1. PRBS_CFG_1 (Address = 0x0119) [Reset = 0x0574]

Bit	Field	Type	Reset	Description
15:13	Reserved	R	0x0	
12	Send_Packet	R/W	0x0	Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set
11	Reserved	R	0x0	
10:8	CFG_PRBS_CHK_SEL	R/W	0x5	000: Checker receives from RGMII TX 010: Checker receives from RMII TX 011: Checker receives from MII TX 101: Checker receives from Cu RX
7	Reserved	R	0x0	
6:4	CFG_PRBS_GEN_SEL	R/W	0x7	000: PRBS transmits to RGMII RX 010: PRBS transmits to RMII RX 011: PRBS transmits to MII RX 101: PRBS transmits to Cu TX

Table 8-1. PRBS_CFG_1 (Address = 0x0119) [Reset = 0x0574] (continued)

Bit	Field	Type	Reset	Description
3	CFG_PRBS_CNT_Mode	R/W	0x0	1b = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0b = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting.
2	CFG_PRBS_CHK_Enable	R/W	0x1	Enable PRBS checker xbar (to receive data). Must be enabled for packet counters to work
1	CFG_PKT_GEN_PRBS	R/W	0x0	If bit[1] is set: (a) When pkt_gen_en is set, PRBS packets are generated continuously (b) When pkt_gen_en is cleared, PRBS RX checker is still enabled If bit [1] is cleared: (a) When pkt_gen_en is set, non - PRBS packet is generated (b) When pkt_gen_en is cleared, PRBS RX checker is disabled as well
0	PKT_GEN_Enable	R/W	0x0	1b = Enable packet/PRBS generator 0b = Disable packet/PRBS generator

8.2 PRBS_STATUS_4 (Address = 0x011F) [Reset = 0x0000]

Table 8-2. PRBS_STATUS_4 (Address = 0x011F) [Reset = 0x0000]

Bit	Field	Type	Reset	Description
15:14	Reserved	R	0x0	
13	PRBS_Sync_Loss	R/WoC	0x0	1b = PRBS has locked 0b = PRBS has not locked
12	Pkt_Done	R	0x0	Set when all MAC packets with CRC are transmitted
11	Pkt_Gen_Busy	R	0x0	1b = Packet generator is in process 0b = Packet generator is not in process
10	PRBS_Pkt_Ov	R	0x0	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[1] of 0x011F
9	PRBS_Byte_Ov	R	0x0	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit[1] of 0x011F
8	PRBS_Lock	R	0x0	1b = PRBS checker is locked (sync) on received byte stream 0b = PRBS checker is not locked
7:0	PRBS_Err_Cnt	R	0x0	Holds number of errored bits received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

9 USB to MDIO Procedure

Follow this procedure when using the USB to MDIO GUI for the 510 EVM application:

1. Follow the general USB to MDIO userguide:
2. Change the extended register to No.

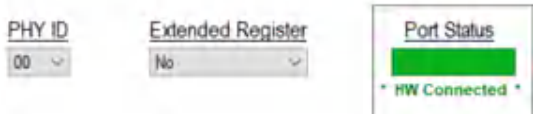

Figure 9-1. Example of Changing Extended Register to NO

3. Use 000D and 000E for extended register.

2.4 Vpp with Extended Register Example:

```
//Set Output operating mode for 2.4 Vpp
begin
000D 0001
000E 08F6
000D 4001
000E 1000 //enable 2.4 Vpp operating mode

000D 0007
000E 020E
000D 4007
000E B000 //Request increased the transmit level in MMD07

000D 001F
000E 0010
000D 401F
000E 4000 //soft reset
end
```

1V Vpp with Extended Register Example:

```
//Set Output operating mode for 1V Vpp
begin
000D 0001
000E 08F6
000D 4001
000E 0000 //enable 1 Vpp operating mode

000D 0007
000E 020E
000D 4007
000E 8000 //Do not request increased transmit level in MMD07

000D 001F
000E 0010
000D 401F
000E 4000 //soft reset
end
```

10 IEEE 802.3cg PMA Compliance

The DP83TD510E is IEEE 802.3cg 10Base-T1L compliant. The device supports all the required test modes within the standard for assessing PHY compliance.

When testing the PMA compliance of the DP83TD510E, it is necessary to configure the PHY into the appropriate test mode. The IEEE 802.3cg specifies three test modes to measure the transmitter's waveform, distortion, jitter, and droop. The IEEE 802.3cg standard specifies limits for both 1.0 Vpp and 2.4 Vpp output operating modes.

Table 10-1. IEEE 802.3cg 10Base-T1L PMA Specifications

Test		Limit	
		1.0 Vpp mode	2.4 Vpp mode
Output Voltage	Maximum	1.05 mV	2.520 mV
	Minimum	0.850 mV	2.040 mV
Droop	Positive	10%	10%
	Negative	10%	10%
Jitter		10 ns	
PSD	Mask	Template	Template
	Power Level	-0.2 – 2.2 dBm	7.4 – 9.8 dBm

The default output operating mode will be 1.0 Vpp without a link partner detected. Select the output operating mode of the DP83TD510E by running the script below for 2.4 Vpp in the 1-V and 2.4-V p2p mode session for the test mode 1, 2, and 3.

```
//Set Output operating mode for 2.4 Vpp for test mode 1,2,and 3
begin
000D 0001
000E 08F6
000D 4001
000E 1000 //force 2.4V

000D 001F
000E 0016
000D 401F
000E 0104 //enable digital loopback to force link up to have three level signal
end
```

1. Test Mode 1: Transmitter output voltage and timing jitter test mode.
   a. When the DP83TD510E is configured in test mode 1, the PHY repeats the data sequence (+1, -1).

```
begin
000d 0001
000e 08f8
000d 4001
000e 2000 //Set test mode 1 in MMD 01
001f 4000 //soft reset
end
```

2. Test Mode 2: Transmitter output droop test mode.
   a. When the DP83TD510E is enabled in test mode 2, the PHY repeats ten "+1" symbols followed by ten "-1" symbols.

```
begin
000d 0001
000e 08f8
000d 4001
000e 4000 //Set test mode 2 in MMD 01
001f 4000 //soft reset
end
```

3. Test Mode 3: Normal operation in Idle mode, to be used in PSD Mask tests.
   a. Test mode 3 sets the DP83TD510E in the MDI master mode transmitting normal Inter-Frame idle signals.

```
begin
000d 0001
000e 08f8
000d 4001
000e 6000 //Set test mode 1 in MMD 01
001f 4000 //soft reset
end
```

4. MDI Return Loss for slave mode: Slave Idle mode.
   a. 1V p2p MDI Return Loss compliance test.

```
begin

//001f 8000 //hard reset

000d 0007
000e 0200
000d 4007
000e 0000 //disable autoneg MMD 07

000d 0001
000e 0834
000d 4001
000e 0000 //Force Slave Mode MMD 01

000d 0001
000e 08f6
000d 4001
000e 0000 //Force 1V swing MMD 01

001f 4000 //soft reset

end
```

   b. 2.4-V p2p MDI Return Loss compliance test.

```
begin

//001f 8000 //hard reset

000d 0007
000e 0200
000d 4007
000e 0000 //disable autoneg MMD 07

000d 0001
000e 0834
000d 4001
000e 0000 //Force Slave Mode MMD 01

000d 0001
000e 08f6
000d 4001
000e 1000 //Force 2.4V swing MMD 01

001f 4000 //soft reset

end
```

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2022) to Revision C (June 2022)	Page
• Updated the 2.4V script for PMA compliance test and Added MDI Return Loss compliance test script	17

Changes from Revision A (June 2021) to Revision B (May 2022)	Page
• Added 1-V and 2.4-V p2p mode scripts	4
• Updated script for TDR test and add a additional note for TDR test on High attenuation cable	6
• Updated the ALCD script. Added the note on maximum calibration range,	7
• Change the register in the script from 09AF to 0A9F, Adding note on 2.4V script give better performance on ALCD	10
• Changed the 2.4V script for PMA compliance	17

Changes from Revision * (March 2021) to Revision A (June 2021)	Page
• Updated 0x1E register writes for TDR start	6
• Updated register definition to correspond to data sheet	6
• Added USB to MDIO Procedure section	16

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265