PRACTICAL CONSIDERATIONS FOR IMPLEMENTING PoDL-COUPLING CIRCUITS

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ABSTRACT

PoDL coupling circuit has critical impact on the operational parameters in single-pair Ethernet applications. It must meet many opposing and challenging requirements, that affect:

a) Link quality (e.g. Return Loss, balance)

b) Power-related parameters (losses, max. current and voltage)

c) Temperature rating and size of components

Presented material describes the challenges and approach to designing PoDL-coupling circuits with considerations to all critical parameters. The material is generic, but also includes some considerations related directly to 100BASE-T1 application as well as to low-power PoDL, 3W PD with 12V PSE.

OBJECTIVES

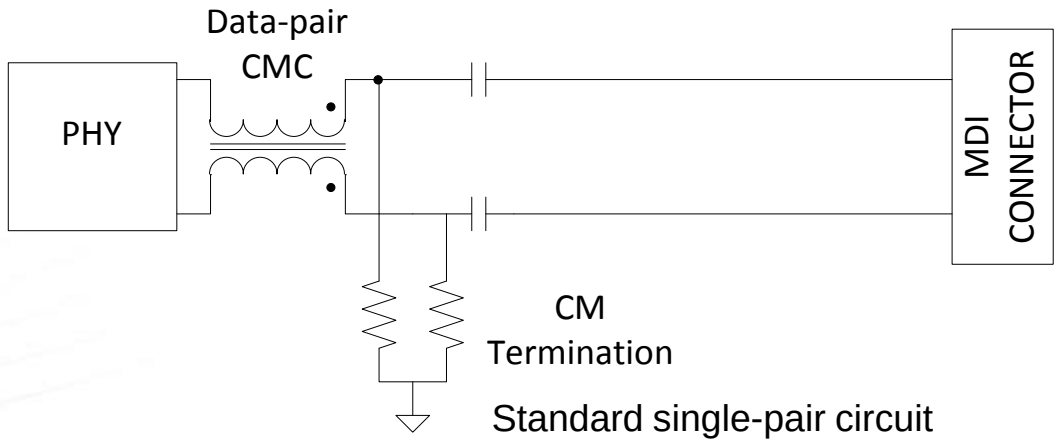
- Critically consider PoDL-coupling circuit, irrespective of the data-rate and bandwidth.
- Detail the critical parameters and how to assess their effects.
- Present material in a way that can be adopted for any PoDL option and bandwidth.
- Provide an insight in what the circuit might have to meet for 100BASE-T1 application and for low-power application using 12V PSE.

OPERATIONAL CONSIDERATIONS

WITH 100BASE-T1 EXAMPLE

STANDARD MDI CONFIGURATION

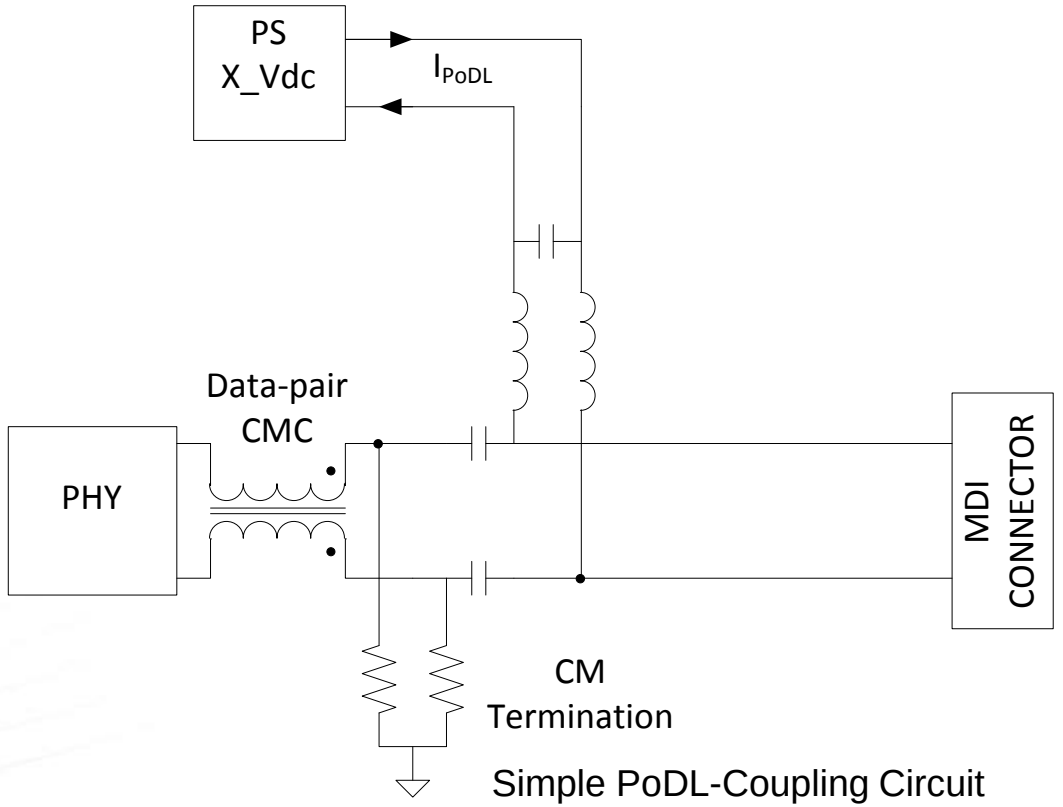
- Data-line CMC, rated <100mA and about 5Ω per line (based on 100 Mbps).
- Optional resistors for common-mode termination.
- DC-block capacitors, no need for Safety-rated isolation.



ADDING PoDL-COUPLING INDUCTORS TO STANDARD MDI

- Power-coupling inductors MUST HAVE:
  - Sufficient inductance to meet the minimum RL requirement at low operating frequencies
  - High-enough SRF to meet the minimum RL requirement at high operating frequencies
  - Low enough DCR to avoid excessive DC-voltage drop

- The circuits on the PSE and PD sides are identical.



Simple PoDL-Coupling Circuit

SIMPLE PoDL-COUPLING CIRCUIT: BASIC CHALLENGES

- Meeting trade-off between contradicting requirements for
  - Sufficiently high L (favors more turns, larger size)
  - High SRF (favors fewer turns, smaller size)
  - High I_{BIAS} and saturation (favors larger size and fewer turns)
  - Low DCR (favors thicker wires and fewer turns)
  - Minimizing size of the package

- Degradation at high temperatures – harder-to-find stable core materials may be required for operation at high temperatures, e.g. 105C and 125C.

- Meeting the listed trade-offs is challenging, especially in 100BASE-T1 applications and where space is very tight, e.g. small automotive cameras.

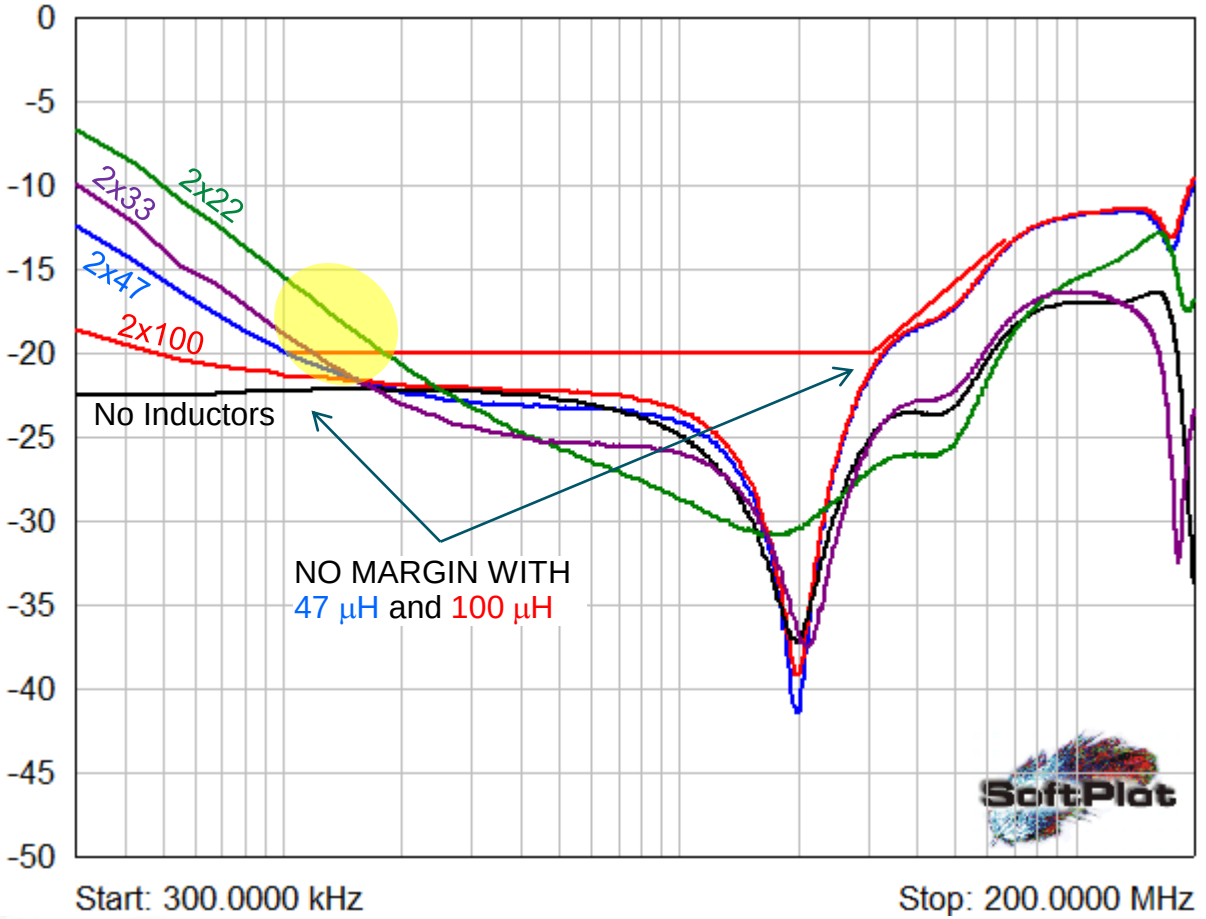
EXAMPLE: INDUCTOR-PARAMETERS FOR 100BASE-T1 APPLICATION

- Well-established performance requirements for 100BASE-T1 single-pair Ethernet were used.
- Various inductors have been connected in pairs “across” the MDI lines to emulate the added impedance of the PoDL coupling inductors.
- Sdd11 (negative Return-Loss) was measured to determine the effect of the inductors.
- RL measurements have been done with “passive” connection of the components, no PoDL.

- Results help define the minimum requirements for inductors under worst-case conditions.
- In real application, the used components have to meet the established parameters across the entire DC-bias and temperature range.

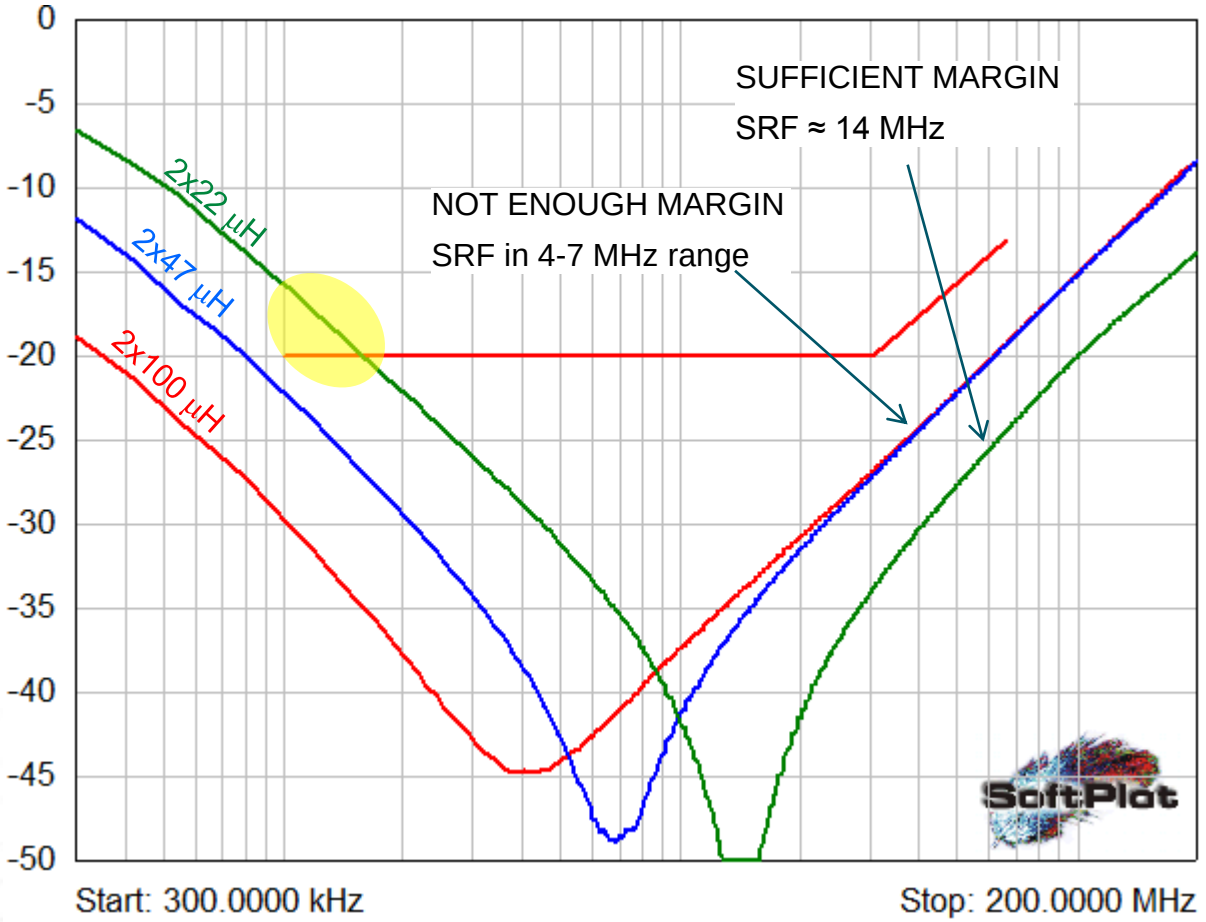
EFFECT OF INDUCTORS ADDED IN PARALLEL TO 100 Mbps DATA PAIR

- 100BASE-T1 non-PoDL MDI -RL limit line shown as red line.
- Measured Sdd11 on:
  - Original unmodified PCB with 100 Mbps MDI
  - PCB with added: 2x22 μH, 2x33 μH, 2x47 μH, 2x100 μH (photo)
  - 100 μH & 47 μH in larger package than 33 μH & 22 μH
- Inductors degrade the MDI RL.
  - 2x47 μH and 2x100 μH - pass with no margin.
  - 2x22 μH - fail under 1.8 MHz, otherwise have good margin.



RL OF INDUCTORS-ONLY

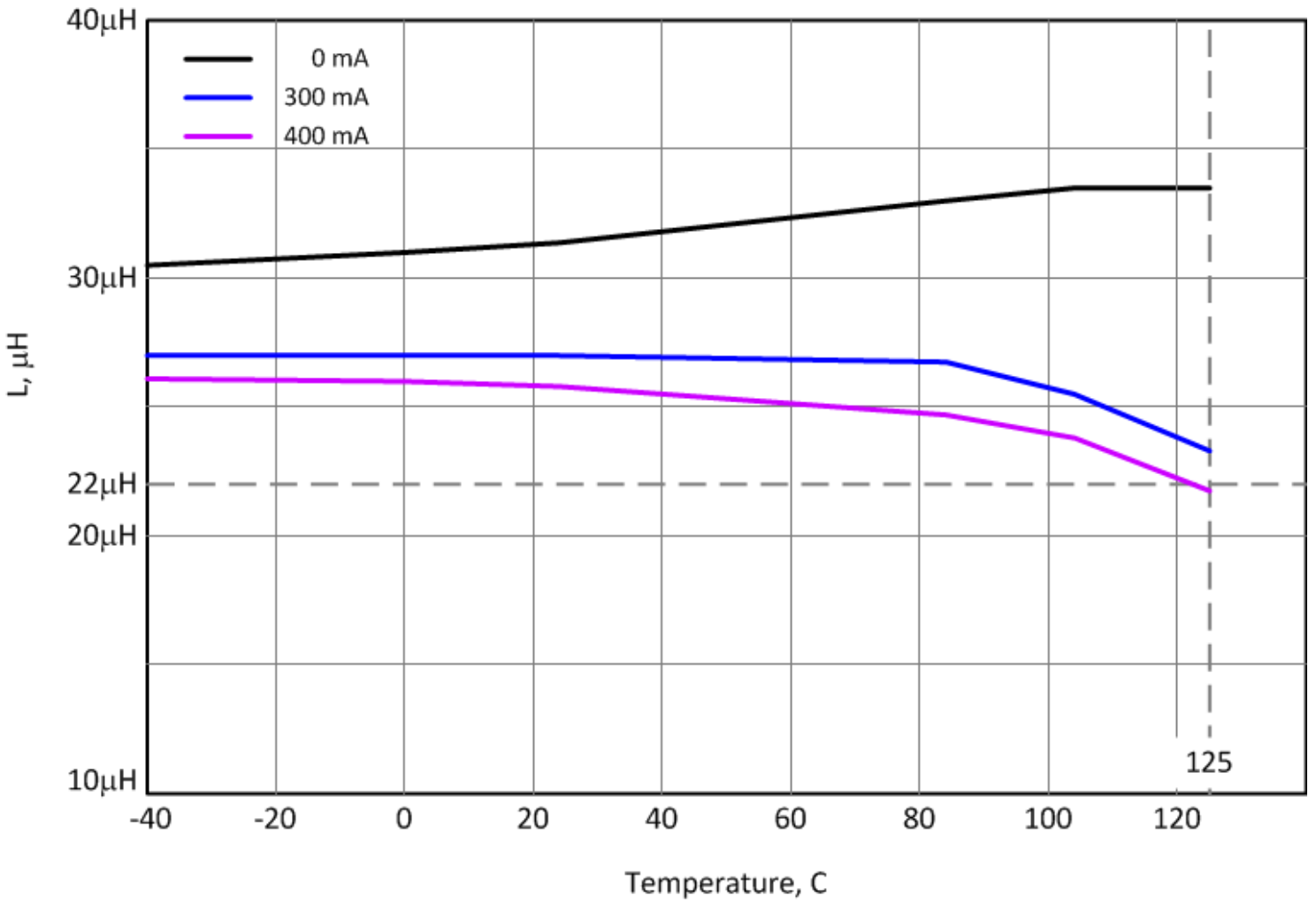
- Inductors on a test jig, each “leg” terminated 50Ω to “GND”.
- Larger margin from the non-PoDL MDI RL limit is needed to account for degradation due to other MDI components.



INDUCTANCE vs. TEMPERATURE vs. DC BIAS

- Inductance degrades with T and I_{BIAS}.
- Combined WORST-CASE is critical to determine suitability of inductors.
- Inductors must not degrade below the MINIMUM required L under combined worst-case operating conditions.

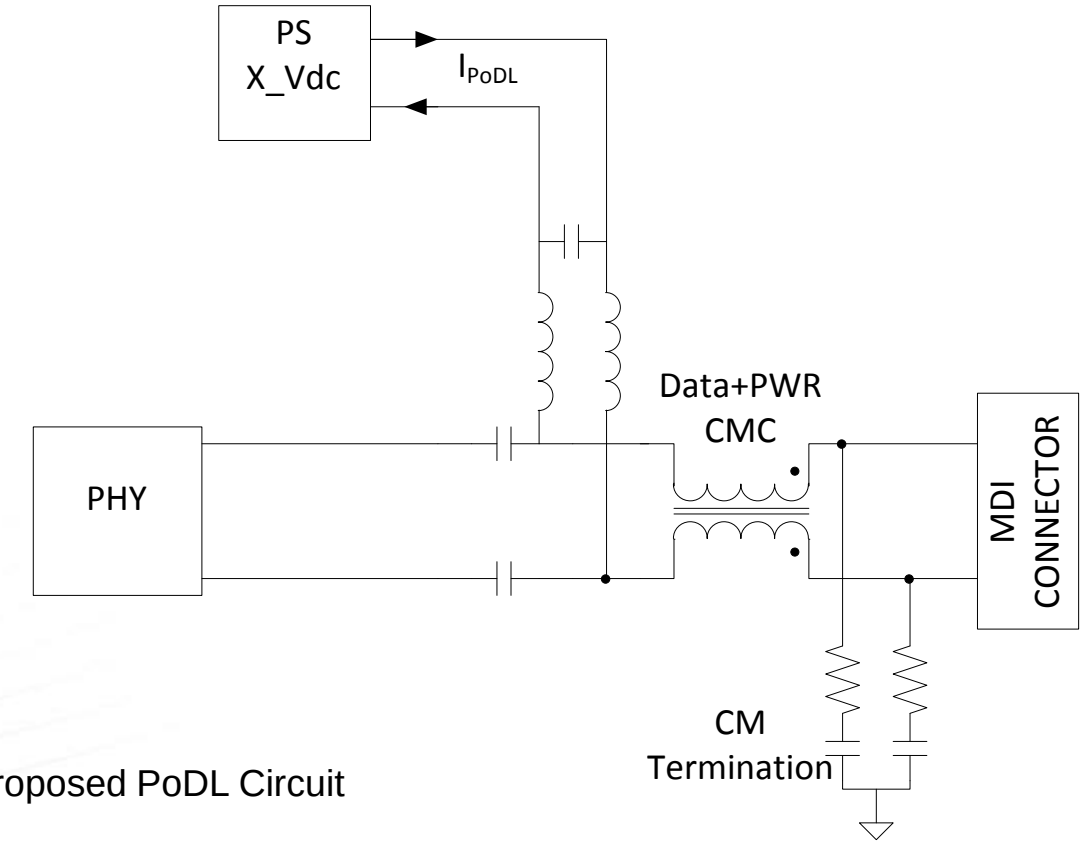
- Example shows measured data for an inductor with the following parameters:
  - Nominal 33 μH, 3.2 mm x 2.5 mm x 2.5 mm
  - DCR_{125C}<0.6Ω
- E.g. if the minimum required L=22 μH, the measured inductor is suitable for nearly 400 mA and up to 125C.
- If the minimum L=27 μH, the same inductor can operate with 300 mA up to 85C.



PROPOSED CIRCUIT

- A properly designed CMC can suppress the effects of conversion by the inductors.
- The figure shows a proposed circuit over UTP:
  - A CMC is placed between the MDI connector and the coupling inductors.
  - CM termination circuit is on the line side of the CMC.
  - CM termination is DC-blocked.
- The CMC adds to the DCR and power-losses.

- The required CMC characteristics:
  - Sufficient CM-CM rejection
  - Sufficiently high balance (low conversion)
  - Meet the RL/TDR impedance requirements
  - Meet the Insertion-Loss requirements
  - Sufficient current and temperature ratings
  - Low-enough DCR
  - Acceptable size

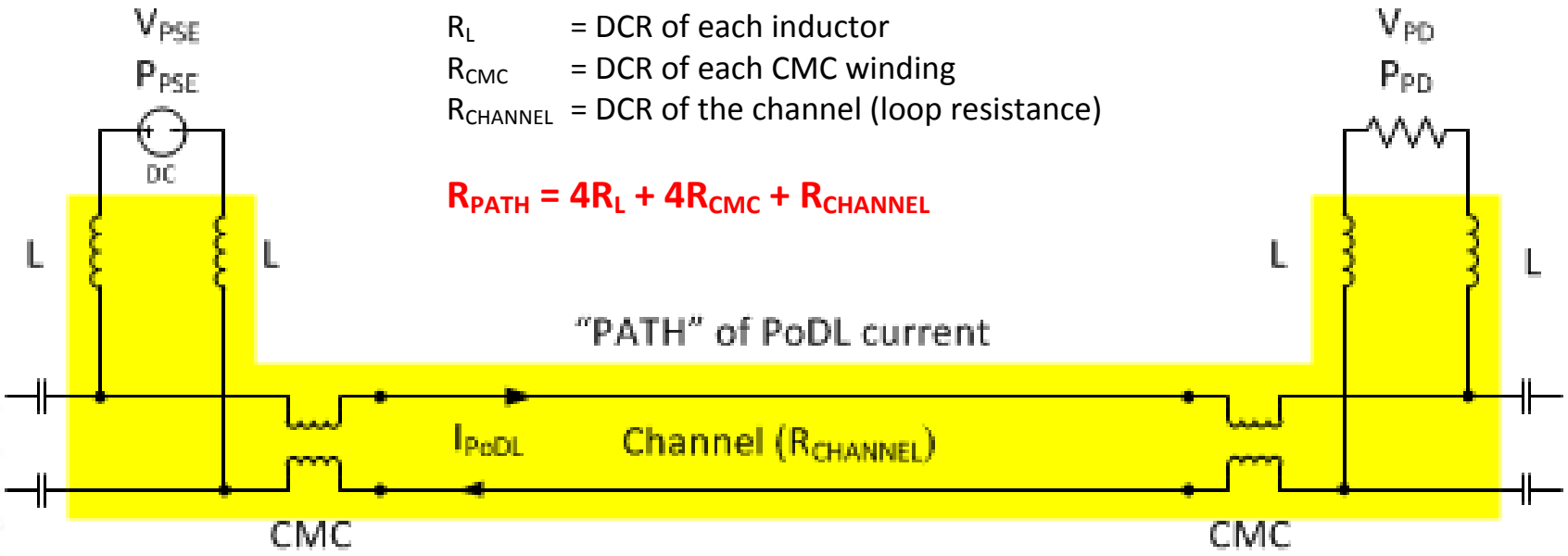


Proposed PoDL Circuit

DC CONSIDERATIONS

WITH STABLE-12V PSE AND 3W PD EXAMPLE

PoDL-CURRENT PATH AND DC PARAMETERS



- I_{PoDL} must not cause excessive voltage drop over the DCR in the entire PoDL path
- V_{PD} must be sufficiently high to provide the required power P_{PD}.

- Power available to PD: $\mathbf{P_{PD} = I_{PoDL} \times V_{PSE} - I_{PoDL}^2 \times R_{PATH}}$

EXAMPLE DC CALCULATIONS: STABLE-12V PSE AND 3W PD

- For 20% power-margin:

$I_{PoDL} x V_{PSE} = 1.2P_{PD}$

$I_{PoDL}^2 \times R_{PATH} = 0.2P_{PD}$

PoDL current= $I_{PoDL} = 1.2P_{PD}/V_{PSE} = 1.2x3/12 = 0.3A$

Maximum DCR= $\mathbf{R_{PATH}} = 0.2P_{PD}/I_{PoDL}^2 = \mathbf{6.7\Omega}$

- R_L and R_{CMC} must have a DCR that is only a fraction of an Ohm to meet the requirements of this example.

- For 50% power-margin:

$I_{PoDL} x V_{PSE} = 2P_{PD}$

PoDL current= $I_{PoDL} = 2P_{PD}/V_{PSE} = 2x3/12 = 0.5A$

Maximum DCR= $R_{PATH} = P_{PD}/I_{PoDL}^2 = \mathbf{12\Omega}$

- The maximum R_{PATH} requirement must be met up to the highest operating temperature.
- Power-supply circuits may require additional components that may further increase R_{PATH}.

$$R_{PATH} = 4R_L + 4R_{CMC} + R_{CHANNEL}$$

SUGGESTIONS FOR CONSIDERATIONS

- Range of inductors wrt. the required characteristics (L, SRF, DCR, size).
  Determine the minimum inductance that allows reliable operation for the data-rate.
- Range of CM chokes wrt. the required characteristics (impedance, balance, DCR, size).
- PoDL electrical/MDI specification in light of practically attainable parameters.
  Consider the necessary parameters and margins and if possible allow for trade-offs.
- PoDL power-classification (power, voltage, current) in light of practical DC considerations.
  Keep in mind practically attainable components, their DCR, sizes, and other characteristics, and how they affect power available to PD.

END